

08/30/00 U.S. PTO

9-01-00 A

PTO/SB/05 (4/98)

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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. MI 22-1332

First Inventor or Application Identifier Honeycutt

Title Transistor Structures, Methods of...

Express Mail Label No. F1 465687187

1234567890

08/30/00

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

1.  \* Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2.  Specification [Total Pages 24]
  - Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3.  Drawing(s) (35 U.S.C. 113) [Total Sheets 9]
4. Oath or Declaration [Total Pages 3]
  - a.  UNEXECUTED Newly executed (original or copy)
  - b.  Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed)
    - i.  DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

**\* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).**

ADDRESS TO: Assistant Commissioner for Patents  
Box Patent Application  
Washington, DC 20231

5.  Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
  - a.  Computer Readable Copy
  - b.  Paper Copy (identical to computer copy)
  - c.  Statement verifying identity of above copies

**ACCOMPANYING APPLICATION PARTS**

7.  Assignment Papers (cover sheet & document(s))
8.  37 C.F.R. § 3.73(b) Statement  Power of (when there is an assignee)  Attorney
9.  English Translation Document (if applicable)
10.  Information Disclosure Statement (IDS)/PTO-1449  Copies of IDS Citations
11.  Preliminary Amendment
12.  Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
  - \* Small Entity Statement(s)  Statement filed in prior application (PTO/SB/09-12)
  - 13.  Certified Copy of Priority Document(s) (if foreign priority is claimed)
  - 14.  Other: Check # 127747.....

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

 Continuation     Divisional     Continuation-in-part (CIP)    of prior application No: \_\_\_\_\_ / \_\_\_\_\_

Prior application information: Examiner

Group / Art Unit:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICATION FOR LETTERS PATENT**

\* \* \* \*

**Transistor Structures, Methods of Forming  
Transistor Structures, and Methods of Forming  
Insulative Material Against Conductive Structures**

\* \* \* \*

**INVENTORS**

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ATTORNEY'S DOCKET NO. MI22-1332

1 Transistor Structures, Methods of Forming Transistor Structures, and  
2 Methods of Forming Insulative Material Against Conductive Structures

3 **TECHNICAL FIELD**

4 The invention pertains to methods of forming insulative materials  
5 against conductive structures, and in particular aspects pertains to  
6 methods of forming transistor structures. Also, the invention pertains to  
7 transistor structures.

8

9 **BACKGROUND OF THE INVENTION**

10 A frequently used procedure of semiconductor fabrication is  
11 formation of a so-called "self-aligned contact" (SAC) opening. An  
12 exemplary use of a SAC opening is to expose a node between a pair of  
13 wordlines, and can be conducted as follows. First, a pair of adjacent  
14 wordlines are formed over a substrate, and then insulative sidewall  
15 spacers are formed along conductive portions of the lines. The  
16 wordlines typically comprise conductive portions capped by insulative  
17 material. Suitable insulative material for capping the wordlines is silicon  
18 nitride. A thick insulative layer (typically borophosphosilicate glass  
19 (BPSG)) is formed over the wordlines and insulative sidewall spacers.  
20 The insulative sidewall spacers are formed of a material different than  
21 the thick insulative layer, with a suitable material being silicon nitride.

22 An opening is etched through the thick insulative layer and to an  
23 electrical node between the wordlines. If the thick insulative layer

1 comprises BPSG and the sidewall spacers comprise silicon nitride, the  
2 etch utilizes conditions which are selective for the BPSG relative to the  
3 silicon nitride. The insulative spacers are exposed during formation of  
4 the opening, but are etched more slowly than the BPSG, and preferably  
5 are not entirely removed by the etch of the BPSG. The opening is  
6 intended to be formed to have a periphery "aligned" with the spacers,  
7 and the formation of the opening is referred to as a "self-aligned  
8 contact" etch.

9 It is desired that the spacers not be entirely removed during  
10 formation of the opening so that the spacers can protect the conductive  
11 material of the wordlines from being exposed when the opening is  
12 formed. If the conductive material of the wordlines becomes exposed in  
13 the openings, device failure will likely result. A problem with current  
14 semiconductor fabrication processes is that silicon nitride insulative  
15 spacers are occasionally over-etched during formation of contact openings  
16 in BPSG, leading to exposure of wordline conductive material, and to  
17 device failure.

18 A possible method for overcoming the above-discussed problem is  
19 described in U.S. Pat. No. 5,700,349, which suggests utilizing  $\text{Si}_x\text{O}_y\text{N}_z$  or  
20  $\text{Al}_x\text{O}_y$  based materials to protect conductive portions of a wordline during  
21 a SAC method. The utilization of  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_x\text{O}_y$  as protective  
22 materials relative to the conductive material of a wordline during a SAC  
23 method shows promise, in that  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_x\text{O}_y$  appear to be more

1           resistant to SAC etch conditions than is a silicon nitride protective  
2       material. However, the materials of U.S. Pat. No. 5,700,349 have  
3       problems associated with their use, and it would be desirable to  
4       overcome such problems.

5

6       SUMMARY OF THE INVENTION

7           In one aspect, the invention encompasses a method of forming an  
8       insulative material along a conductive structure. A conductive structure  
9       is provided over a substrate, and an electrically insulative material is  
10      formed along at least a portion of the conductive structure. The  
11      electrically insulative material comprises at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  
12       $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater than 0 and less than 10.  
13      A dopant barrier layer is formed over the electrically insulative material.  
14      BPSG is formed over the dopant barrier layer, and the dopant barrier  
15      layer prevents dopant migration from the BPSG to the electrically  
16      insulative material.

17           In another aspect, the invention encompasses methods of forming  
18      transistor structures.

19           In yet another aspect, the invention encompasses a transistor  
20      structure which includes a transistor gate formed over a semiconductive  
21      substrate. The transistor gate has a sidewall which comprises electrically  
22      conductive material. Source/drain regions are within the substrate and  
23      proximate the transistor gate. An electrically insulative material is along

1 the electrically conductive material of the sidewall of the transistor gate.  
2 The electrically insulative material comprises at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  
3  $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater than 0 and less than 10.  
4 A layer consisting of silicon dioxide is over the transistor gate,  
5 electrically insulative material and substrate. A layer of BPSG is over  
6 the layer consisting of silicon dioxide.

7

8 **BRIEF DESCRIPTION OF THE DRAWINGS**

9 Preferred embodiments of the invention are described below with  
10 reference to the following accompanying drawings.

11 Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a  
12 portion of a semiconductor wafer at an initial processing step of a  
13 method of the present invention.

14 Fig. 2 is a view of the Fig. 1 wafer fragment shown at a  
15 processing step subsequent to that of Fig. 1.

16 Fig. 3 is a view of the Fig. 1 wafer fragment shown at a  
17 processing step subsequent to that of Fig. 2.

18 Fig. 4 is a view of the Fig. 1 wafer fragment shown at a  
19 processing step subsequent to that of Fig. 3.

20 Fig. 5 is a view of the Fig. 1 wafer fragment shown at a  
21 processing step subsequent to that of Fig. 4.

1       Fig. 6 is a view of the Fig. 1 wafer fragment shown at a  
2 processing step subsequent to that of Fig. 1 in accordance with a second  
3 embodiment of the present invention.

4       Fig. 7 is a view of the Fig. 6 wafer fragment shown at a  
5 processing step subsequent to that of Fig. 6.

6       Fig. 8 is a view of the Fig. 6 wafer fragment shown at a  
7 processing step subsequent to that of Fig. 7.

8       Fig. 9 is a view of the Fig. 6 wafer fragment shown at a  
9 processing step subsequent to that of Fig. 8.

10

11 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

12       This disclosure of the invention is submitted in furtherance of the  
13 constitutional purposes of the U.S. Patent Laws "to promote the progress  
14 of science and useful arts" (Article 1, Section 8).

15       In one aspect, the invention is a recognition that deposited  
16 antireflective coating (DARC) materials (which are typically  $\text{Si}_x\text{O}_y\text{N}_z$ ,  
17 wherein x, y and z are greater than 0 and less than 10) can be utilized  
18 to protect conductive materials of wordlines during an etch of BPSG  
19 (such as, for example, during a SAC etch).

20       The invention also encompasses a recognition that if  $\text{Si}_x\text{O}_y\text{N}_z$  is  
21 utilized to protect a conductive material during an etch, the  $\text{Si}_x\text{O}_y\text{N}_z$  is  
22 preferably electrically insulative. The  $\text{Si}_x\text{O}_y\text{N}_z$  can then function to

1 prevent shorting between the protected conductive material and other  
2 conductive materials proximate the protected conductive material.

3 Further, the invention encompasses a recognition that  $\text{Si}_x\text{O}_y\text{N}_z$  can  
4 have different characteristics if dopant is provided therein relative to if  
5 the material is undoped. Specifically, if dopant permeates within  $\text{Si}_x\text{O}_y\text{N}_z$ ,  
6 the material can develop conductive characteristics which will destroy its  
7 ability to function as an electrically insulative protective layer. Dopant  
8 can migrate from a doped oxide (such as, for example, BPSG) provided  
9 against  $\text{Si}_x\text{O}_y\text{N}_z$ , and accordingly the invention encompasses provision of  
10 a dopant barrier layer between  $\text{Si}_x\text{O}_y\text{N}_z$  and a doped oxide provided  
11 proximate the  $\text{Si}_x\text{O}_y\text{N}_z$ .

12 Dopant migration problems may also occur relative to materials  
13 comprising  $\text{Al}_p\text{O}_q$  (wherein p and q are greater than 0 and less than 10),  
14 and accordingly the invention also comprises provision of a dopant  
15 barrier layer between materials comprising  $\text{Al}_p\text{O}_q$  and doped oxide (such  
16 as, for example, BPSG).

17 A first embodiment method of the present invention is described  
18 with reference to Figs. 1-5. Referring initially to Fig. 1, a  
19 semiconductor wafer fragment 10 comprises a semiconductive material  
20 substrate 12 having wordlines 14, 16, 18 and 20 formed thereover.  
21 Substrate 12 can comprise, for example, monocrystalline silicon lightly  
22 doped with a background p-type dopant. To aid in interpretation of the  
23 claims that follow, the terms "semiconductive substrate" and

1 “semiconductor substrate” are defined to mean any construction  
2 comprising semiconductive material, including, but not limited to, bulk  
3 semiconductive materials such as a semiconductive wafer (either alone or  
4 in assemblies comprising other materials thereon), and semiconductive  
5 material layers (either alone or in assemblies comprising other materials).  
6 The term “substrate” refers to any supporting structure, including, but  
7 not limited to, the semiconductive substrates described above.

8 Wordlines 14, 16, 18 and 20 comprise a gate oxide layer 22, a  
9 polysilicon layer 24, a silicide layer 26, a silicon dioxide layer 28, and  
10 an insulative cap 30. Gate oxide layer 22 can comprise, for example,  
11 silicon dioxide; semiconductive material layer 24 can comprise, for  
12 example, conductively-doped polysilicon; silicide layer 26 can comprise, for  
13 example, tungsten silicide or titanium silicide; and insulative cap 30 can  
14 comprise, for example, silicon nitride.

15 Shallow trench isolation regions 32 are formed within substrate 12  
16 and electrically isolate at least some of the shown electrical components  
17 of wafer fragment 10 from adjacent circuitry (not shown).

18 Conductively doped diffusion regions 34, 36 and 38 are formed  
19 within substrate 12 and between wordlines 14, 16, 18 and 20.  
20 Wordlines 14, 16, 18 and 20 extend into and out of the page (i.e., are  
21 in the shape of lines extending across a top of substrate 12), and paired  
22 diffusion regions are formed within substrate 12 at spaced intervals along  
23 the wordlines. The portions of the wordlines which gatedly connect pairs

1 of diffusion regions constitute transistor gates. Accordingly, the shown  
2 portion of wordline 16 constitutes a transistor gate between diffusion  
3 regions 34 and 36, and the shown portion of wordline 18 constitutes a  
4 transistor gate between diffusion regions 36 and 38.

5 Diffusion regions 34, 36 and 38 can be doped with one or both  
6 of n-type dopant and p-type dopant, and can comprise halo regions  
7 and/or lightly doped diffusion (Ldd) regions for transistor structures  
8 formed from gates 16 and 18.

9 Wordlines 14, 16, 18 and 20 comprise sidewalls 15, 17, 19 and 21,  
10 respectively, with portions of the sidewalls defined by layers 24 and 26  
11 comprising conductive portions. A silicon dioxide layer 40 is formed  
12 along the conductive portions of sidewalls 15, 17, 19 and 21, as well as  
13 over diffusion regions 34, 36 and 38. Silicon dioxide layer 40 can be  
14 formed by, for example, exposing wafer fragment 10 to oxidizing  
15 conditions. Such oxidation can correspond to so-called "smiling gate"  
16 oxidation which is known in the art to improve performance of transistor  
17 devices. In particular embodiments of the invention which are not  
18 shown, layer 40 can be eliminated (e.g., not formed).

19 Referring to Fig. 2, a pair of layers 42 and 44 are formed over  
20 wordlines 14, 16, 18 and 20, as well as over regions of substrate 12  
21 between wordline 14, 16, 18 and 20. Layers 42 and 44 comprise  
22 electrically insulative material, and at least one of layers 42 and 44  
23 comprises at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  (silicon oxynitride) and  $\text{Al}_p\text{O}_q$ , with p,

1 q, x, y and z being greater than 0 and less than 10. Layers 42 and 44  
2 can further comprise other insulative materials such as, for example,  
3 silicon nitride (which typically is  $\text{Si}_3\text{N}_4$ ). Each of layers 42 and 44 can  
4 have a thickness of, for example, from about 10Å to about 750Å, with  
5 a suitable thickness being about 150Å. In embodiments in which layer  
6 40 is not formed (not shown), layer 42 will physically contact (i.e., be  
7 against) the conductive material of wordlines 14, 16, 18 and 20.

8 In particular embodiments, one of layers 42 and 44 can consist of  
9 either  $\text{Si}_x\text{O}_y\text{N}_z$  or  $\text{Al}_p\text{O}_q$  (or consist essentially of such materials), and the  
10 other of layers 42 and 44 can consist of silicon and nitrogen (or consist  
11 essentially of silicon and nitrogen), and can be, for example,  $\text{Si}_3\text{N}_4$ .  
12 Alternatively, one of layers 42 and 44 can consist of aluminum and  
13 oxygen (or consist essentially of such materials), and the other of layers  
14 42 and 44 can consist of silicon and nitrogen (or consist essentially of  
15 such materials). In yet another alternative embodiment, one of layers  
16 42 and 44 can consist of silicon, nitrogen and oxygen (or consist  
17 essentially of such materials), and the other of layers 42 and 44 can  
18 consist of silicon and nitrogen (or consist essentially of such materials).  
19 An exemplary material which consists of aluminum and oxygen  $\text{Al}_2\text{O}_3$ .

20 Referring to Fig. 3, layers 42 and 44 are anisotropically etched to  
21 form electrically insulative pillars 45, 47, 49 and 51 along sidewalls 15,  
22 17, 19 and 21, respectively. A suitable anisotropic etch of materials 42  
23 and 44 can comprise, for example, a plasma etch utilizing one or more

1 of CF<sub>4</sub>, CHF<sub>3</sub> and O<sub>2</sub>. The anisotropic etch of layers 42 and 44  
2 removes such layers from over wordlines 14, 16, 18 and 20.

3 Although in the shown embodiment pillars 45, 47, 49 and 51 are  
4 spaced from conductive portions of sidewalls 15, 17, 19 and 21 by silicon  
5 oxide layer 40, it is to be understood that the invention encompasses  
6 other embodiments (not shown) wherein oxide material 40 is not formed,  
7 and accordingly wherein pillars 45, 47, 49 and 51 are formed against the  
8 conductive portions of sidewalls 15, 17, 19 and 21. Also, although in  
9 the shown embodiment the anisotropic etching of materials 42 and 44 is  
10 selective relative to the silicon oxide material 40 such that oxide  
11 material 40 is not etched by the anisotropic etching conditions, it is to  
12 be understood that the invention encompasses other embodiments (not  
13 shown) wherein oxide material 40 is removed by the anisotropic etching  
14 conditions. Additionally, the invention encompasses embodiments in  
15 which oxide material 40 is removed in an etch subsequent to the  
16 anisotropic etch of materials 42 and 44.

17 Heavily doped source/drain regions 50, 52 and 54 are implanted  
18 proximate gates 16 and 18, utilizing pillars 45, 47, 49 and 51 as spacers  
19 to align the implants. Regions 50, 52 and 54 are referred to as "heavily  
20 doped" regions because they are more heavily doped than regions 34, 36  
21 and 38. A typical peak dopant concentration in regions 50, 52 and 54  
22 is greater than 10<sup>19</sup> atoms/cm<sup>3</sup>. The implanted dopant utilized to form  
23 heavily doped source/drain regions 50, 52 and 54 can be either p-type

1 dopant or n-type dopant, depending on whether PMOS or NMOS  
2 transistors are formed. It is noted that materials 42 and 44 do not  
3 extend over heavily-doped source/drain regions 50, 52 and 54.

4 Although source/drain regions 50, 52 and 54 are shown implanted  
5 through silicon oxide layer 40, it is to be understood that the invention  
6 encompasses other embodiments (not shown) wherein silicon oxide  
7 layer 40 is removed prior to the implant of regions 50, 52 and 54.

8 Referring to Fig. 4, a dopant barrier layer 60 is formed over  
9 pillars 45, 47, 49 and 51, as well as over wordlines 14, 16, 18 and 20.  
10 Dopant barrier layer 60 can consist of silicon dioxide (or consist  
11 essentially of silicon dioxide), and can be formed by chemical vapor  
12 deposition utilizing tetraethyl orthosilicate (TEOS) as a precursor.  
13 Layer 60 can comprise a thickness of, for example, about 250Å.

14 A doped oxide layer 62 is formed over dopant barrier layer 60,  
15 and can comprise, for example, BPSG. Dopant barrier layer 60 prevents  
16 dopant migration from doped oxide 62 into the  $\text{Si}_x\text{O}_y\text{N}_z$  or  $\text{Al}_p\text{O}_q$   
17 materials of pillars 45, 47, 49 and 51. Barrier layer 60 thus alleviates  
18 problems associated with dopant migrating into such materials and  
19 changing the properties of such materials from electrically insulative to  
20 electrically conductive.

21 Referring to Fig. 5, contact openings 66, 68 and 70 are etched  
22 through layers 60 and 62 to expose upper surfaces of source/drain  
23 regions 50, 52 and 54. Openings 66, 68 and 70 can be formed by

photolithographic processing (i.e., by providing a patterned layer of photoresist over an upper surface of doped oxide 62, and subsequent etching through oxides 40, 60 and 62), or other techniques. Pillars 45, 47, 49 and 51 are utilized to align bottom portions of openings 66, 68 and 70 relative to source/drain regions 50, 52 and 54, and accordingly the formation of openings 66, 68 and 70 constitutes a SAC etch. The  $\text{Si}_x\text{O}_y\text{N}_z$  and/or  $\text{Al}_p\text{O}_q$  of pillars 45, 47, 49 and 51 reduces etching of the pillars relative to that which would occur if the pillars were formed entirely of  $\text{Si}_3\text{N}_4$ . However, as discussed above with reference to Fig. 2, one of layers 42 and 44 can consist essentially of silicon nitride. It can be advantageous to have the innermost of the layers (i.e., layer 42) consist of either  $\text{Si}_x\text{O}_y\text{N}_z$  or  $\text{Al}_p\text{O}_q$ , and the outermost of the layers (i.e., layer 44) consist of silicon nitride, so that if there is some over-etching occurring during the anisotropic etching described with reference to Fig. 3, it will be silicon nitride layer 44 which is removed, rather than the layer of  $\text{Si}_x\text{O}_y\text{N}_z$  or  $\text{Al}_p\text{O}_q$ .

Conductive material 72 is formed within openings 66, 68 and 70 to form electrical contacts to source/drain regions 50, 52 and 54. Conductive material 72 can comprise conductively-doped polysilicon, and/or metal, and can comprise multiple materials, such as, for example, a silicide at a lower portion where it joins the source/drain region and either metal nitride or metal above the silicide. In the shown embodiment, wafer fragment 10 comprises a planarized upper surface 74

1 which can be formed by, for example, chemical-mechanical planarization  
2 after filling openings 66, 68 and 70 with conductive material 72.

3 Another embodiment of the invention is described with reference  
4 to Figs. 6-9. In referring to Figs. 6-9, similar numbering will be utilized  
5 as was used above in describing Figs. 1-5, where appropriate.

6 Referring first to Fig. 6, a wafer fragment 100 comprises a  
7 substrate 12 having wordlines 14, 16, 18 and 20 formed thereover. An  
8 insulative material 102 is provided over wordlines 14, 16, 18 and 20, as  
9 well as over regions of substrate 12 between wordlines 14, 16, 18  
10 and 20. Material 102 consists of, or consists essentially of,  $\text{Si}_x\text{O}_y\text{N}_z$  or  
11  $\text{Al}_p\text{O}_q$ , with p, q, x, y and z being greater than 0 and less than 10, and  
12 can be provided to a thickness of, for example, from about 10 $\text{\AA}$  to  
13 about 750 $\text{\AA}$ , with a suitable thickness being greater than about 50 $\text{\AA}$ , and  
14 being, for example, about 25% of the gate length for the particular  
15 structure. In embodiments in which layer 40 is not formed (not shown),  
16 material 102 will contact conductive material of gates 14, 16, 18 and 20.  
17

Referring to Fig. 7, material 102 is anisotropically etched to form  
insulative pillars 104, 106, 108 and 110 adjacent wordlines 14, 16, 18  
and 20, respectively. Subsequently, source/drain regions 50, 52 and 54  
are implanted into substrate 12.

Referring to Fig. 8, a dopant barrier layer 60 and doped oxide  
layer 62 are provided over wordlines 14, 16, 18 and 20 as well as over  
pillars 104, 106, 108 and 110.

Referring to Fig. 9, openings 66, 68 and 70 are formed through materials 40, 60 and 62 to source/drain regions 50, 52 and 54, and such openings are filled with conductive material 72. The formation of openings 66, 68 and 70 can be accomplished by the processing described above with reference to Fig. 5, and accordingly can constitute a SAC etch. Pillars 104, 106, 108 and 110 protect conductive material of wordlines 14, 16, 18 and 20 from being etched during the formation of openings 66, 68 and 70. Further, protective layer 60 (which, as described above, can consist of silicon dioxide and be chemical vapor deposited utilizing TEOS as a precursor), prevents dopant migration from doped oxide 62 into the material of pillars 104, 106, 108 and 110.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1      **CLAIMS:**

2      1. A method of forming an insulative material along a  
3      conductive structure, comprising:

4                providing a conductive structure over a substrate;  
5                forming an electrically insulative material along at least a portion  
6      of the conductive structure, the electrically insulative material comprising  
7      at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater  
8      than 0 and less than 10;

9                forming a dopant barrier layer over the electrically insulative  
10     material; and

11               forming a doped oxide material over the dopant barrier layer, the  
12     dopant barrier layer preventing dopant migration from the doped oxide  
13     material to the electrically insulative material.

14  
15      2. The method of claim 1 wherein the electrically insulative  
16     material is formed to a thickness of at least about 50Å.

17  
18      3. The method of claim 1 wherein the electrically insulative  
19     material consists essentially of the  $\text{Si}_x\text{O}_y\text{N}_z$ .

1       4. The method of claim 1 wherein the electrically insulative  
2 material consists essentially of the  $\text{Si}_x\text{O}_y\text{N}_z$  and is against the conductive  
3 structure.

4  
5       5. The method of claim 1 wherein the electrically insulative  
6 material consists essentially of the  $\text{Al}_p\text{O}_q$ .

7  
8       6. The method of claim 1 wherein the electrically insulative  
9 material consists essentially of the  $\text{Al}_p\text{O}_q$  and is against the conductive  
10 structure.

11  
12       7. The method of claim 1 wherein the forming the dopant  
13 barrier layer comprises chemical vapor depositing silicon oxide from a  
14 TEOS precursor.

15  
16       8. The method of claim 1 wherein the doped oxide material  
17 comprises BPSG.

1           9. A method of forming a transistor structure, comprising:  
2           forming a transistor gate over a substrate, the transistor gate  
3           comprising a sidewall which comprises electrically conductive material;  
4           forming an electrically insulative material along the electrically  
5           conductive material of the transistor gate sidewall; the electrically  
6           insulative material comprising at least two separate layers; the at least  
7           two layers having different chemical compositions from one another; a  
8           first of the at least two layers comprising at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  or  
9            $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater than 0 and less than 10; a  
10          second of the at least two layers consisting essentially of silicon and  
11          nitrogen; and

12           anisotropically etching the electrically insulative material to form  
13          a spacer along the transistor gate sidewall; the anisotropically etching  
14          comprising etching both of the first and second of the at least two  
15          layers.

16  
17           10. The method of claim 9 further comprising implanting a  
18          dopant into the substrate and utilizing the spacer to align the dopant  
19          during the implant.

1        11. The method of claim 9 wherein the first of the at least two  
2 layers is between the second of the at least two layers and the transistor  
3 gate sidewall.

4

5        12. The method of claim 9 wherein the first of the at least two  
6 layers consists essentially of the  $\text{Si}_x\text{O}_y\text{N}_z$  and is between the second of  
7 the at least two layers and the transistor gate sidewall.

8

9        13. The method of claim 9 wherein the first of the at least two  
10 layers consists essentially of the  $\text{Al}_p\text{O}_q$  and is between the second of the  
11 at least two layers and the transistor gate sidewall.

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1           14. A method of forming a transistor structure, comprising:  
2           forming a transistor gate over a substrate, the transistor gate  
3           comprising a sidewall which comprises electrically conductive material;  
4           forming source/drain regions within the substrate and proximate the  
5           transistor gate;  
6           forming an electrically insulative material along the electrically  
7           conductive material of the transistor gate sidewall, the electrically  
8           insulative material comprising at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_p\text{O}_q$ , wherein  
9           p, q, x, y and z are greater than 0 and less than 10;  
10          chemical vapor depositing silicon oxide over the transistor gate and  
11          electrically conductive material utilizing a TEOS precursor; and  
12          forming BPSG over the silicon oxide, the BPSG being spaced from  
13          the electrically insulative material of the spacer by the silicon oxide.

14  
15          15. The method of claim 14 wherein the electrically insulative  
16          material is formed to extend across a top of the transistor gate.

17  
18          16. The method of claim 14 wherein the electrically insulative  
19          material consists of  $\text{Al}_2\text{O}_3$ .

20  
21          17. The method of claim 14 wherein the electrically insulative  
22          material consists of aluminum and oxygen.

1        18. The method of claim 14 wherein the electrically insulative  
2 material consists of silicon, nitrogen and oxygen.

3

4        19. A method of forming a transistor structure, comprising:  
5              forming a transistor gate over a substrate, the transistor gate  
6 comprising a sidewall which comprises electrically conductive material;  
7              forming an electrically insulative material along the electrically  
8 conductive material of the transistor gate sidewall, the electrically  
9 insulative material comprising at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_p\text{O}_q$ , wherein  
10 p, q, x, y and z are greater than 0 and less than 10;  
11              anisotropically etching the electrically insulative material to form  
12 a spacer along the transistor gate sidewall;  
13              implanting a dopant into the substrate and utilizing the spacer to  
14 align the dopant during the implant;  
15              chemical vapor depositing silicon oxide over the transistor gate and  
16 spacer utilizing TEOS as a precursor of the silicon oxide; and  
17              forming BPSG over the silicon oxide, the BPSG being spaced from  
18 the electrically insulative material of the spacer by the silicon oxide.

1       20. The method of claim 19 wherein the electrically insulative  
2 material comprises to different layers that are against one another, one  
3 of the layers consisting of silicon nitride, and the other of the two layers  
4 consisting of either the  $\text{Si}_x\text{O}_y\text{N}_z$  or the  $\text{Al}_p\text{O}_q$ .

5

6       21. A transistor structure, comprising:  
7           a semiconductive substrate;  
8           a transistor gate over the substrate, the transistor gate having a  
9           sidewall which comprises electrically conductive material;  
10          source/drain regions within the substrate and proximate the  
11          transistor gate;  
12          an electrically insulative material along the electrically conductive  
13          material of the sidewall, the electrically insulative material comprising at  
14          least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater  
15          than 0 and less than 10;  
16          a layer consisting of silicon dioxide over the transistor gate,  
17          electrically insulative material, and substrate; and  
18          a layer of BPSG over the layer consisting of silicon dioxide.

19

20       22. The structure of claim 21 wherein the electrically insulative  
21          material extends across a top of the transistor gate.

1       23. The structure of claim 21 wherein the electrically insulative  
2 material does not extend across a top of the transistor gate.

3

4       24. The structure of claim 21 wherein the electrically insulative  
5 material does not extend across a top of the source/drain regions.

6

7       25. The structure of claim 21 wherein the electrically insulative  
8 material consists of aluminum and oxygen.

9

10      26. The structure of claim 21 wherein the electrically insulative  
11 material consists of  $\text{Al}_2\text{O}_3$ .

12

13      27. The structure of claim 21 wherein the electrically insulative  
14 material consists of silicon, nitrogen and oxygen.

15

16      28. The structure of claim 21 wherein the electrically insulative  
17 material comprises a layer of silicon nitride against a layer of the  
18  $\text{Si}_x\text{O}_y\text{N}_z$ .

19

20      29. The structure of claim 21 wherein the electrically insulative  
21 material comprises a layer of silicon nitride against a layer of the  $\text{Al}_p\text{O}_q$ .

1           30. A transistor structure, comprising:

2           a substrate;

3           a transistor gate over the substrate, the transistor gate having a

4           sidewall which comprises electrically conductive material;

5           source/drain regions within the substrate and proximate the

6           transistor gate;

7           an electrically insulative pillar along the electrically conductive

8           material of the sidewall, the pillar comprising a first material against a

9           second material, one of the first and second materials comprising at least

10          one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater than 0

11          and less than 10;

12          a layer consisting of silicon dioxide over the transistor gate, pillar

13          and substrate; and

14          a layer of BPSG over the layer consisting of silicon dioxide.

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16          31. The structure of claim 30 wherein the first material is silicon

17          nitride and the second material is silicon oxynitride.

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1 **ABSTRACT OF THE DISCLOSURE**

2 The invention encompasses a method of forming an insulative  
3 material along a conductive structure. A conductive structure is  
4 provided over a substrate, and an electrically insulative material is  
5 formed along at least a portion of the conductive structure. The  
6 electrically insulative material comprises at least one of  $\text{Si}_x\text{O}_y\text{N}_z$  and  
7  $\text{Al}_p\text{O}_q$ , wherein p, q, x, y and z are greater than 0 and less than 10.  
8 A dopant barrier layer is formed over the electrically insulative material.  
9 BPSG is formed over the dopant barrier layer, and the dopant barrier  
10 layer prevents dopant migration from the BPSG to the electrically  
11 insulative material. The invention also encompasses transistor structures,  
12 and methods of forming transistor structures.

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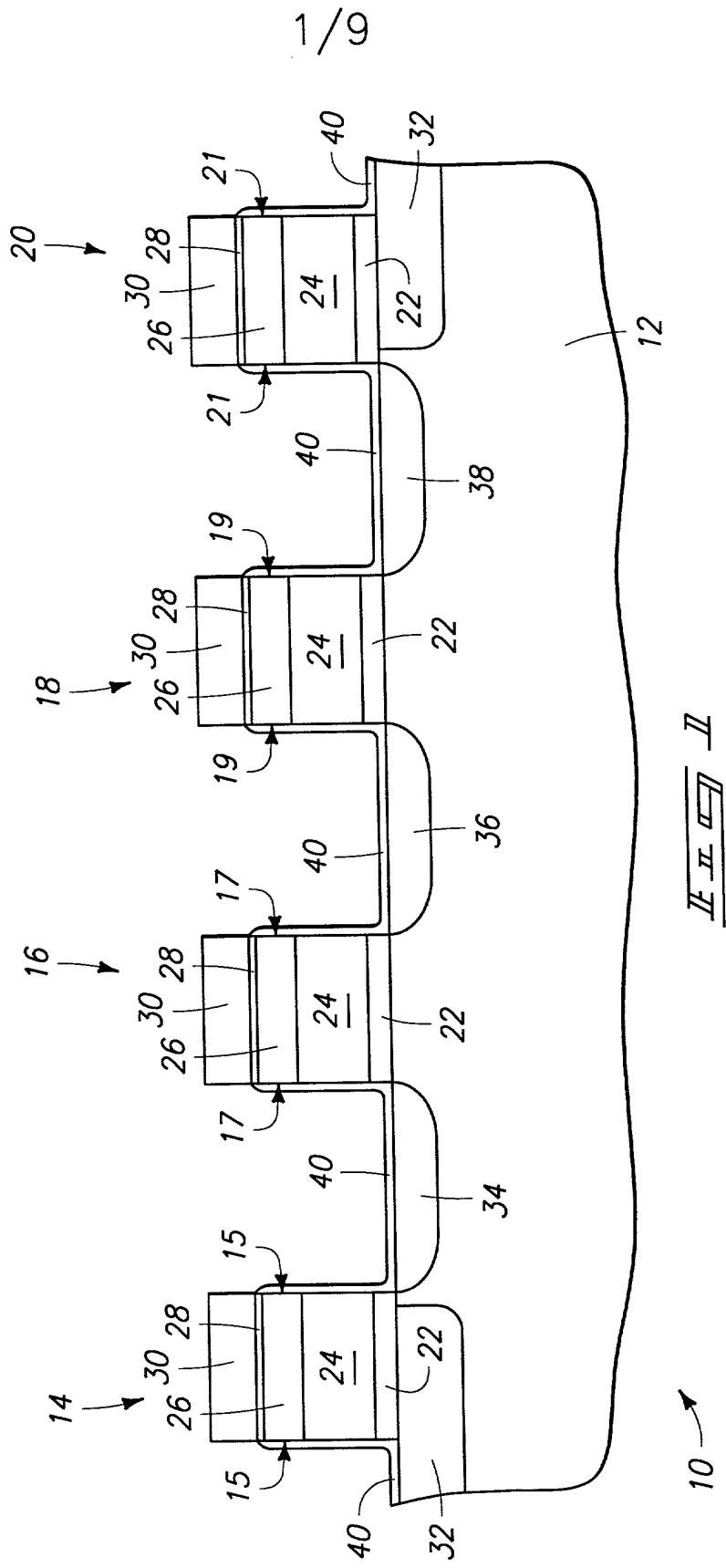
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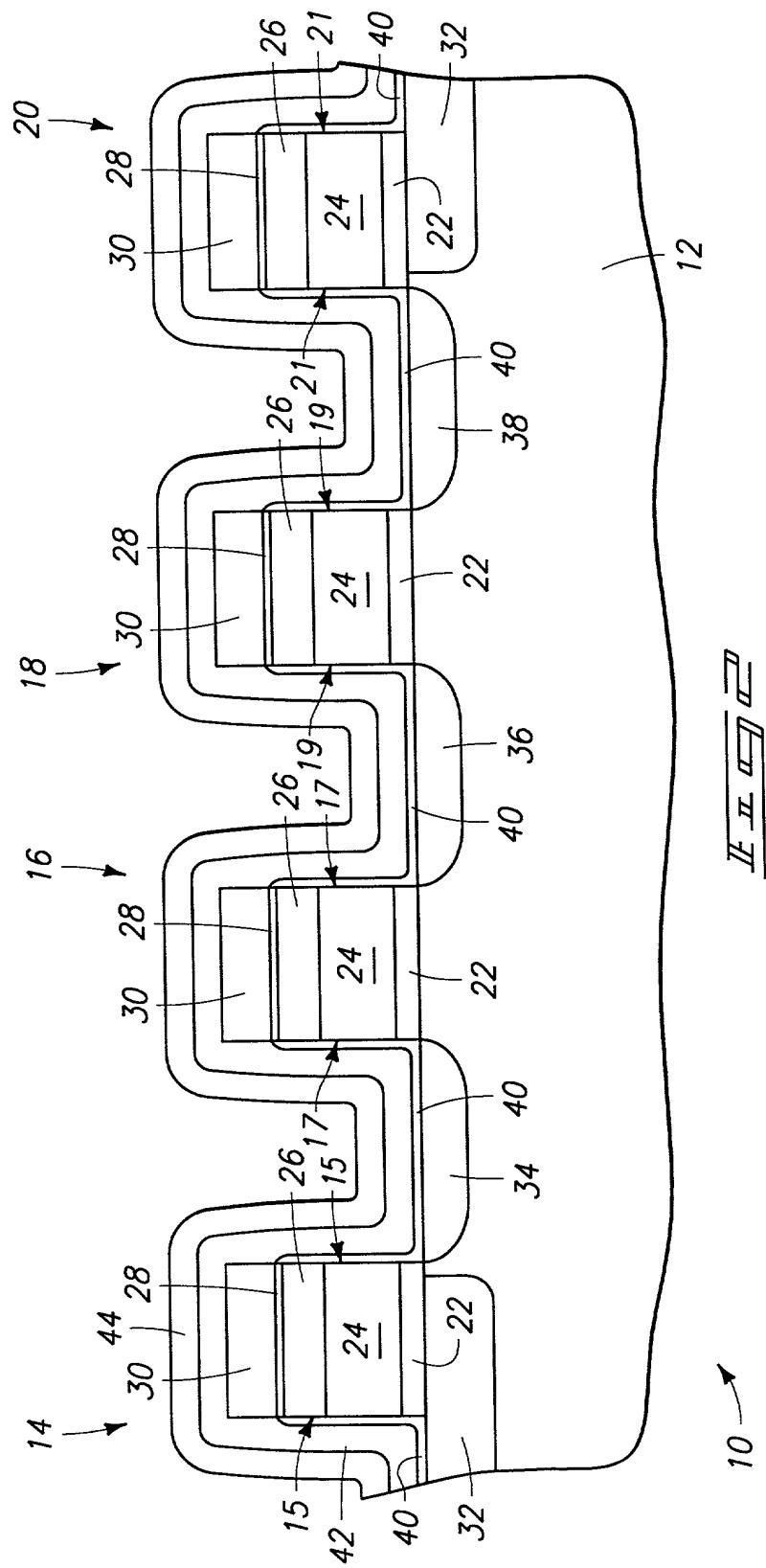
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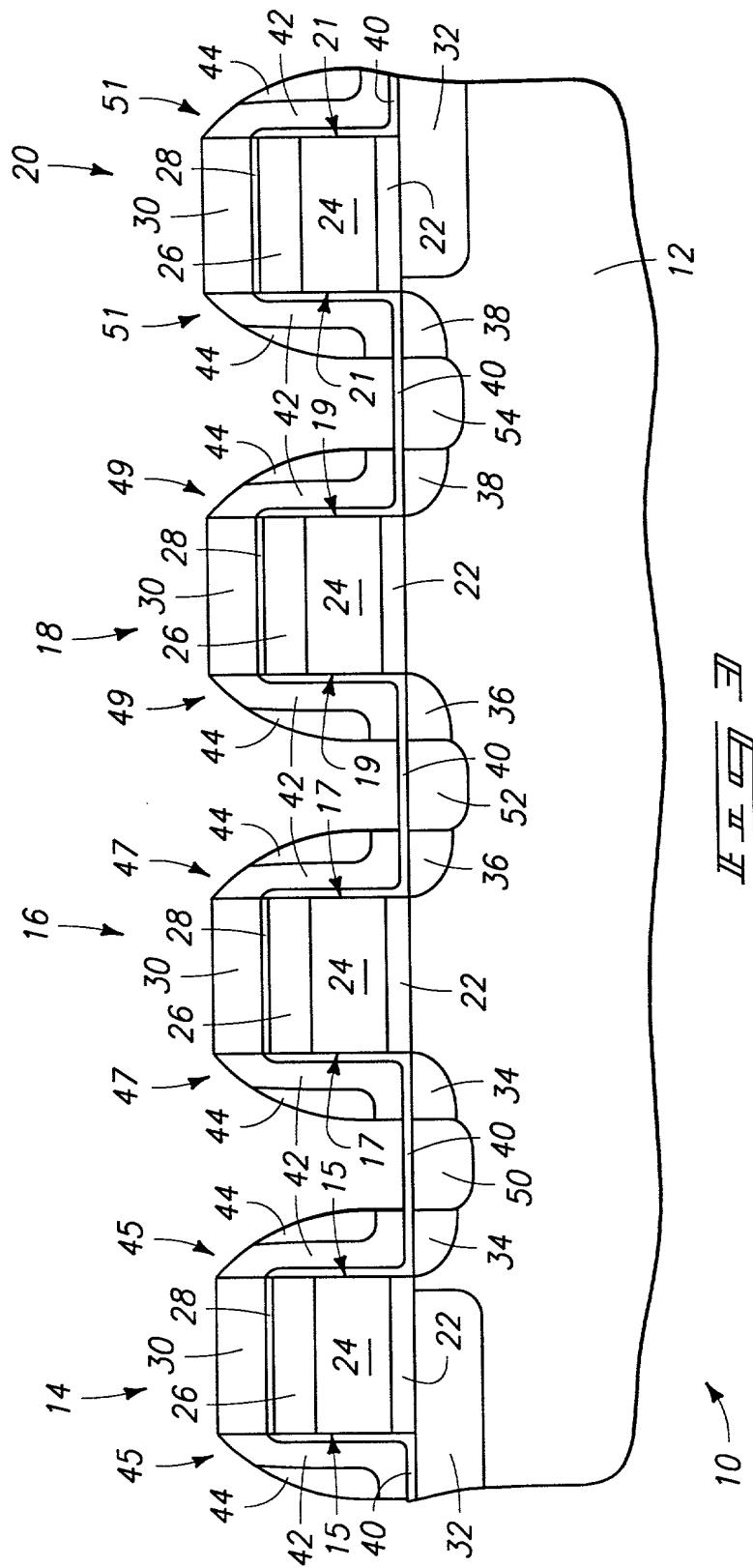
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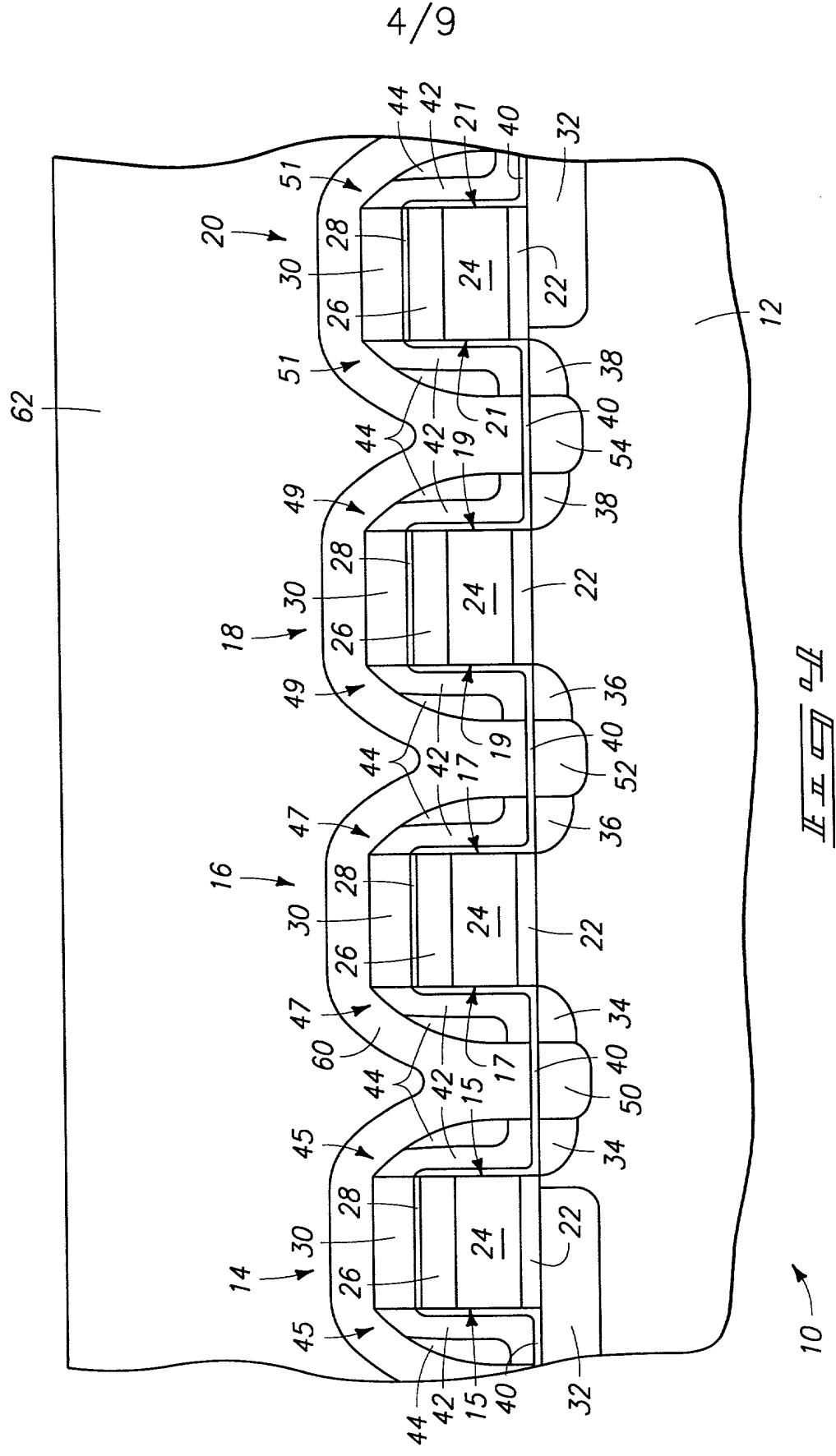


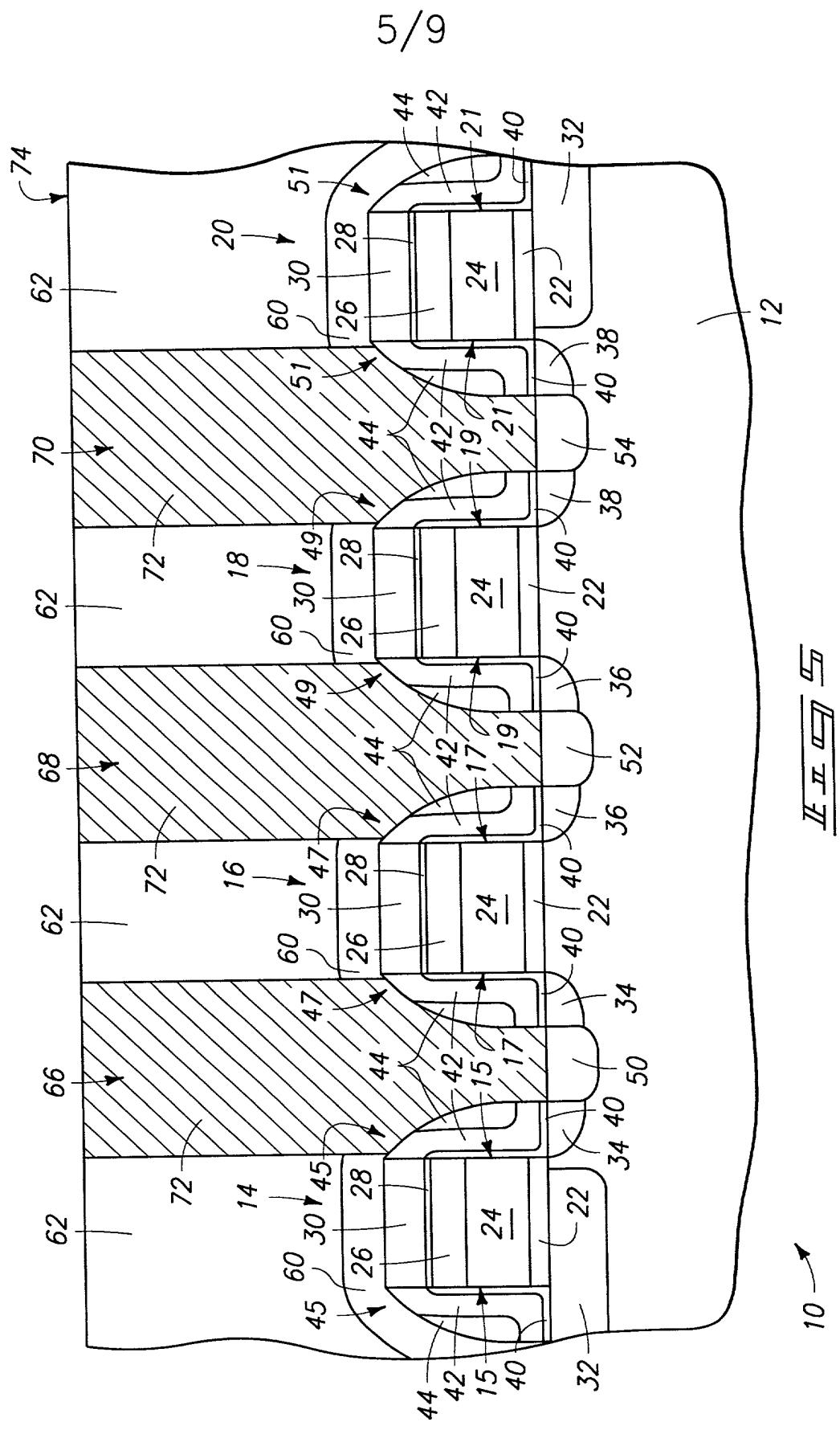
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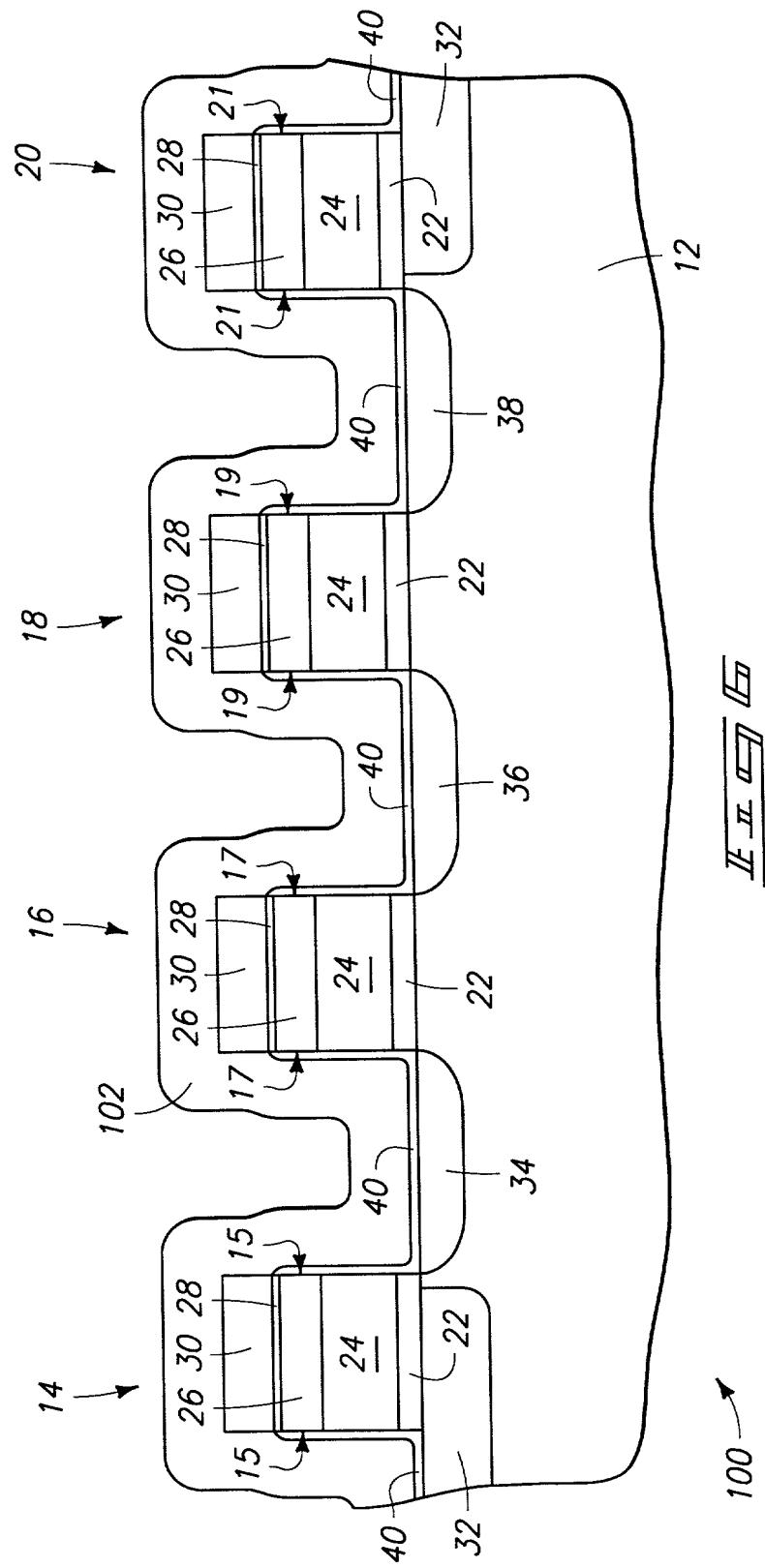
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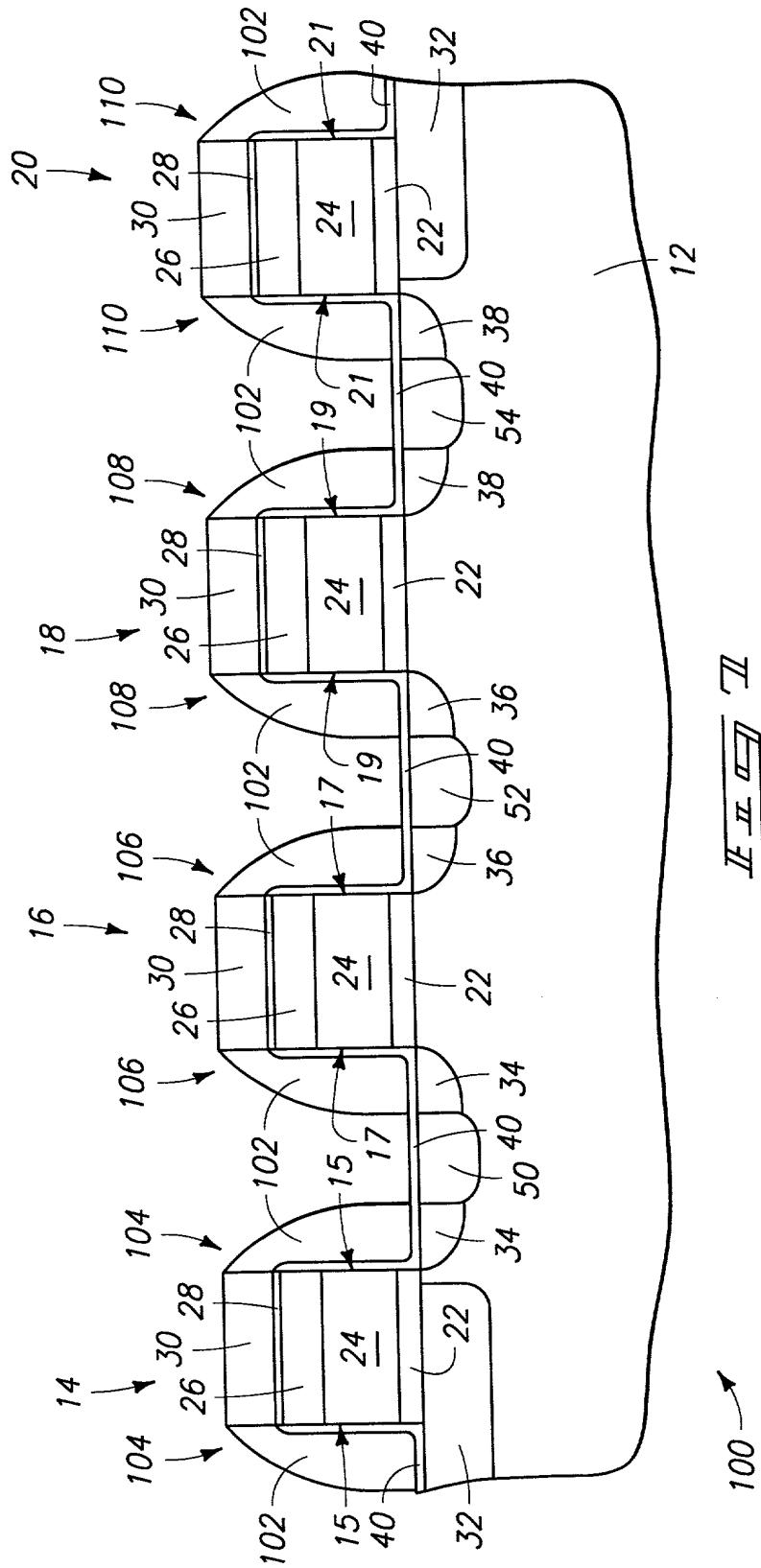


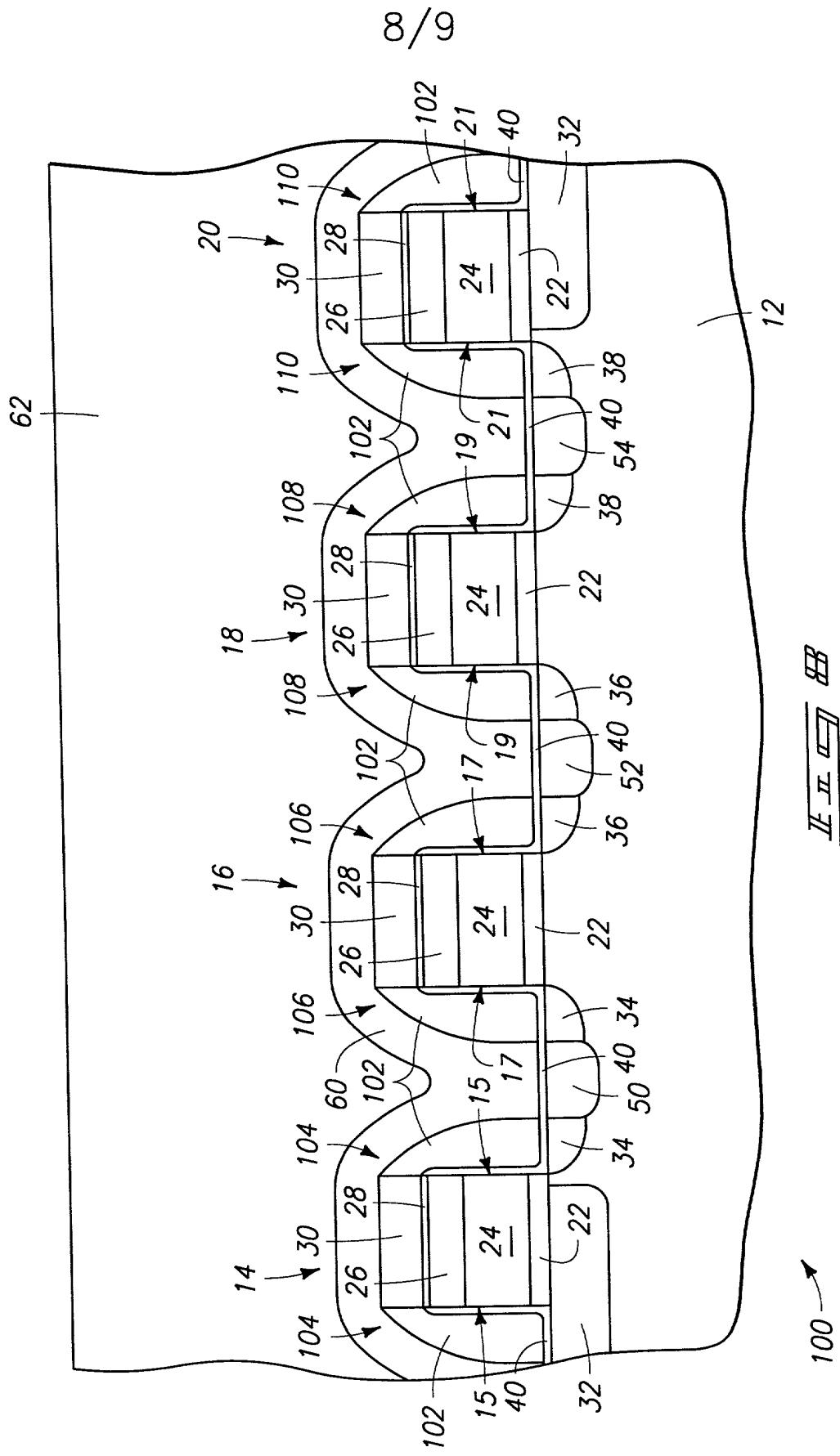


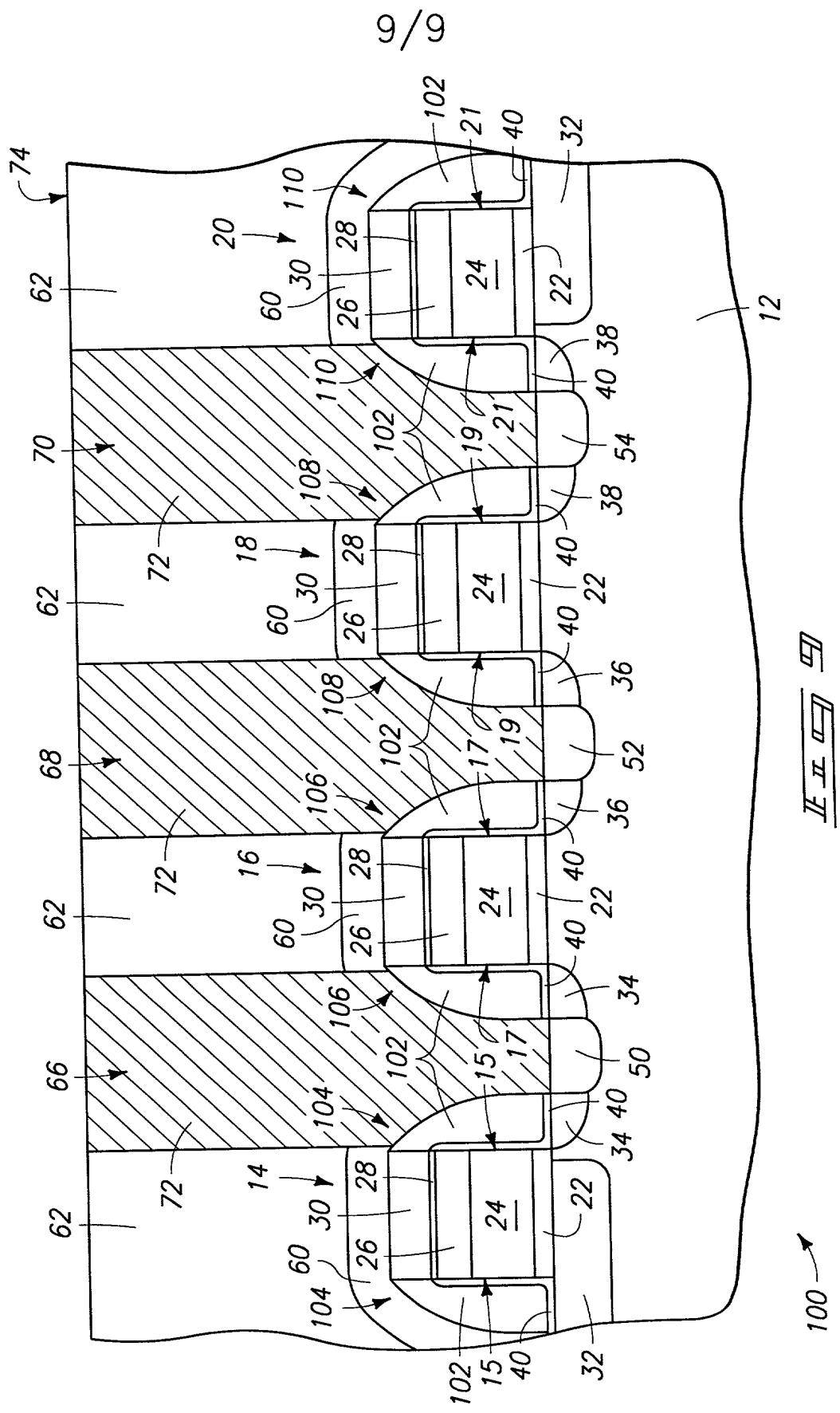
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1            **DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION**

2            As the below named inventor, I hereby declare that:

3            My residence, post office address and citizenship are as stated  
4            below next to my name.

5            I believe I am the original, first and joint inventor of the subject  
6            matter which is claimed and for which a patent is sought on the  
7            invention entitled: Transistor Structures, Methods of Forming Transistor  
8            Structures, and Methods of Forming Insulative Material Against  
9            Conductive Structures, the specification of which is attached hereto.

10          I hereby state that I have reviewed and understand the contents  
11         of the above-identified specification, including the claims.

12          I acknowledge the duty to disclose information known to me to be  
13         material to patentability as defined in Title 37, Code of Federal  
14         Regulations §1.56.

15          **PRIOR FOREIGN APPLICATIONS:**

16          I hereby state that no applications for foreign patents or inventor's  
17         certificates have been filed prior to the date of execution of this  
18         declaration.

19          I hereby declare that all statements made herein of my own  
20         knowledge are true and that all statements made on information and  
21         belief are believed to be true; and further that these statements were  
22         made with the knowledge that willful false statements and the like so

1 made are punishable by fine or imprisonment, or both, under  
2 Section 1001 of Title 18 of the United States Code and that such willful  
3 false statement may jeopardize the validity of the application or any  
4 patent issued therefrom.

5 \* \* \* \* \*

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